The FPS System

communication protocols and data encoding

Version 6.1

This document is written as a result of lengthy discussions with members of the DØ Collaboration and after the Seattle Workshop.

Please read it carefully and send comments/ suggestions to J. Blazey, P. Grannis and M. Martin.

The DØ Collaboration at the Seattle Workshop adopted this final version !!

Manuel J. Martin

August 30, 1999

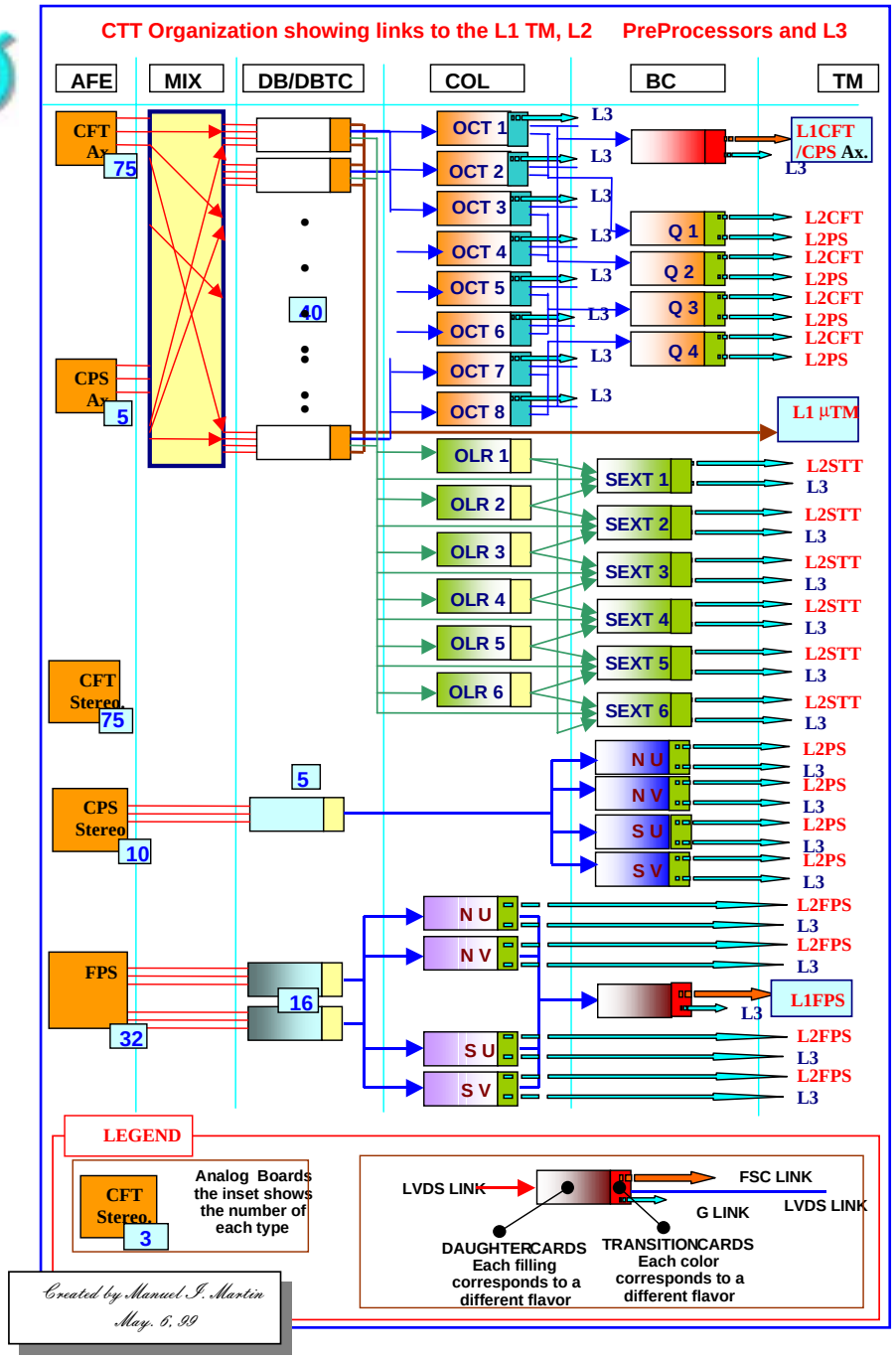


Diagram of the CTT System.

For a better view go to Manuel's Web pages at

http://D0server1.fnal.gov/users/manuel/protocols/diagram.doc

GLOSARY

AFE	Analog Front End Board
MIX	Mixing Box
DB	Digital Board
DBTC	DB Transition Card
COL	Collector Board
BC	BroadCaster Board
TM	Trigger Manager
OCT	COL serving an Octant
Qx	BC serving Quadrant x
OLR	COL serving the Overlapping Regions of the SI match
SEXT	BC covering a Sextant
N/Sx	board serving the North/South side
xU/V	Refers to the U V orientation of the PS strips

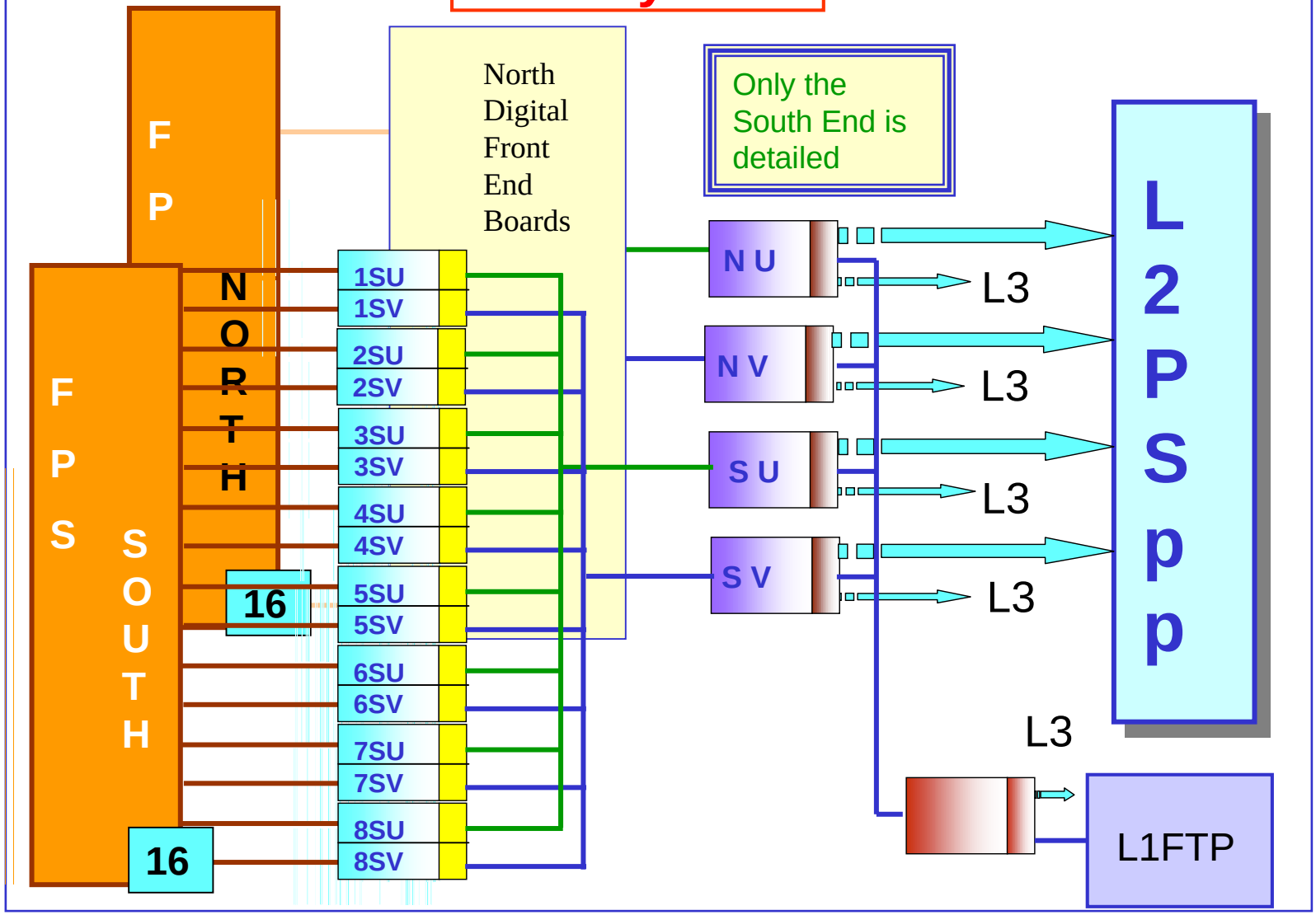
August 30, 1999

L1/L2 FPS

GENERAL

The FPS is organized into two halves: North and South. In turn, each half is organized into an U orientation and a V orientation subset. The output from the four COL boards is sent to the L1 and L2 triggers in the appropriated manner.

FPS System


FPS NORTH
FPS SOUTH
16
16
North Digital Front End Boards
1SU
1SV
2SU
2SV
3SU
3SV
4SU
4SV
5SU
5SV
6SU
6SV
7SU
7SV
8SU
8SV
Only the South End is detailed
N U
N V
S U
S V
L3
L3
L3
L3
L3
L2PSpp
L1FTP

FPS System

FUNCTIONS PERFORMED BY THE BOARDS

DB Front End Digital Board

Collects hits from the FPS and tags them according to their energy threshold level into L or H. Find Clusters in the U and V layers before and after the 'absorber' panel. Match Cluster information according to orientation and threshold. Calculates the number of matched and unmatched tag Clusters and sends this L1 information to the assigned Collector boards. When the L1 Accept is asserted, it send the list of the Clusters found in the "Shower" side and the MIP Pattern associated with it in the corresponding "MIP" layer to the Collector . Information is sent to the COL boards via LVDS links organized by strip orientation. The Maximum number of clusters that each DB can send per LVDS cable is 16. If necessary, the list is truncated by selecting the Clusters with lower address.

COL Collector Board

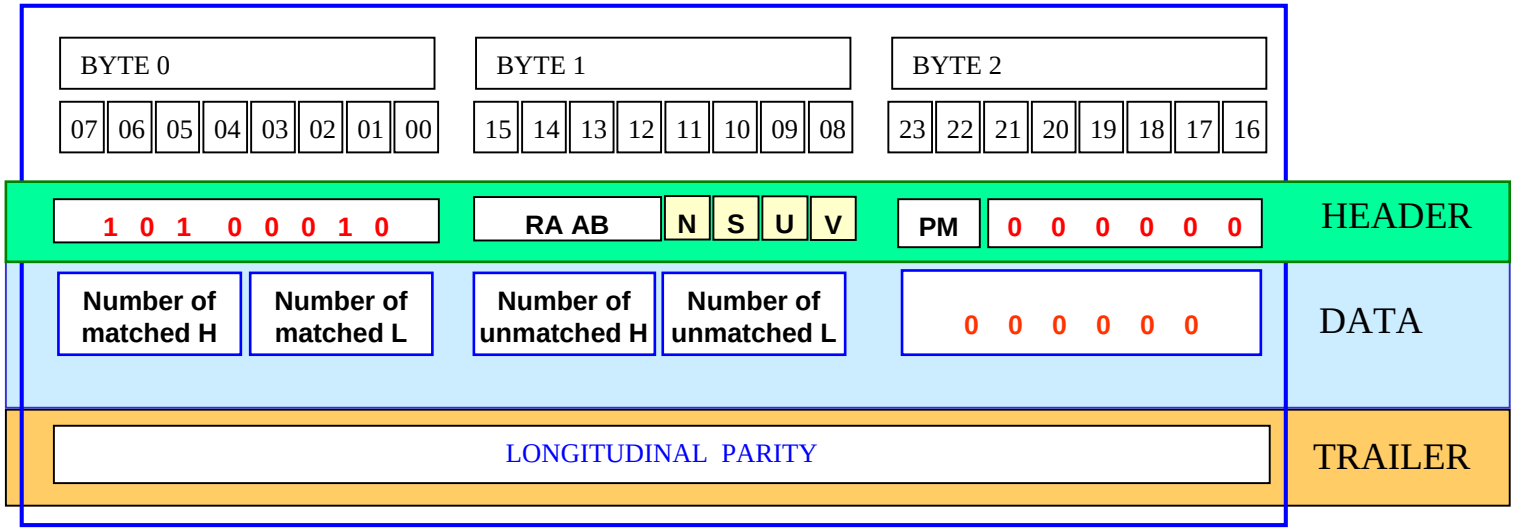
When L1 information arrives, adds the numbers of matched and unmatched Clusters according to their tagging. Sends this information to a BC via LVDS links.

When L2 information arrives, each Collector board merges its eight input lists (Octants North or South) into one selecting U or V information. If the merged lists need to be truncated, priority is given to Clusters with lower address.

BC BroadCaster Board

The Broadcaster board receives L1 information from the four Collectors. It uses this information to create an exhaustive list of up to ninety six Trigger Terms which are sent to a L1FPS Trigger Manager board. The Trigger Manager board selects a subset of 32 terms to be sent to the L1 Trigger.

Bit Fields allocation for L1 FPS data transfers between the Digital Front End boards and the Collector Boards (U/V Boards) using LVDS Links



NOTE Only 2 frames of Data are required
The Maximum number of Matched or Unmatched Clusters reported by type is 16 for a theoretical maximum total of 128.
Clusters are listed ordered in increasing stereo strip index

Bit Fields allocation for L1 FPS data transfers between the Digital Front End boards and the Collector Boards (U/V Boards) using LVDS Links

Frame 1

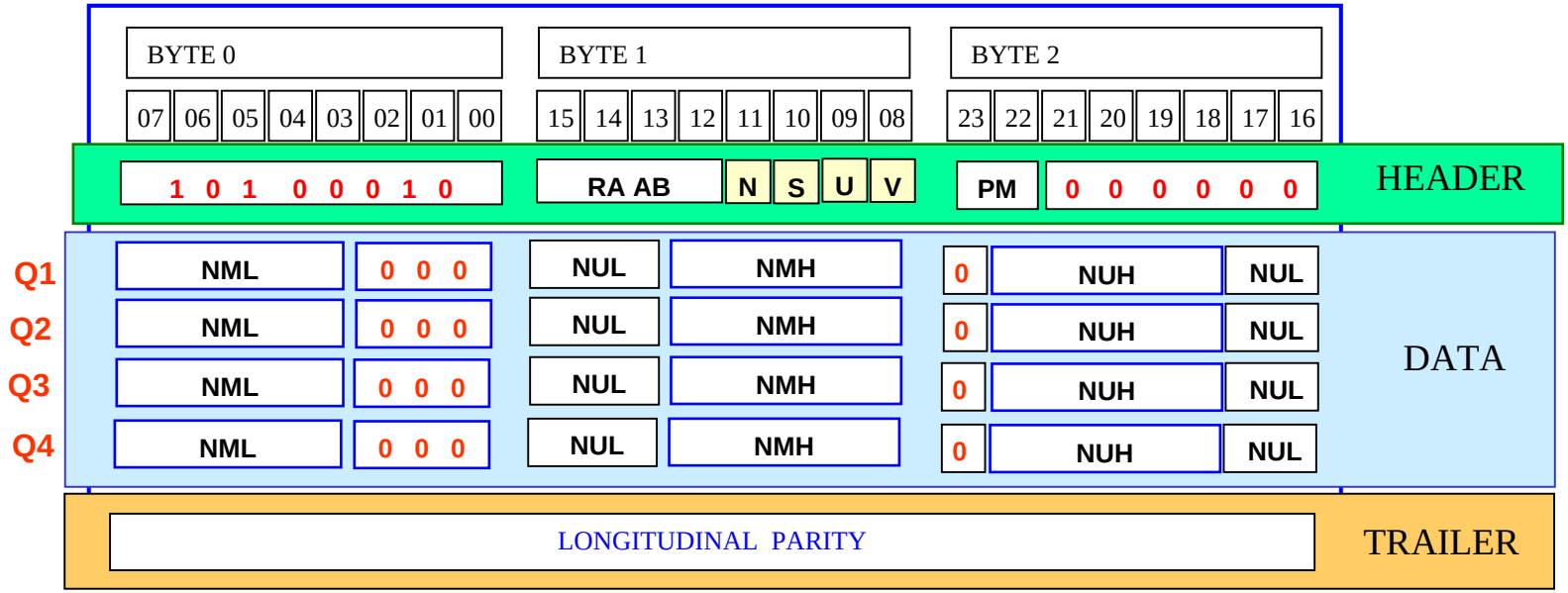
Bits			
[0:7]	Data type	{10100101} = L1FPS	
[8]	Set to 1 if the PS strips have V orientation		
[9]	Set to 1 if the PS strips have U orientation		
[10]	Set to 1 for the South half		
[11]	Set to 1 for the North half		
[12:15]	The Relative Address of Sector in the North/South half		
[16:21]	Null	{000000}	
[22:23]	Pass and Mark	{00}	Normal Data, Normal Event
		{01}	Normal Data, Pass Event (unbiased data)
		{10}	Debug Data Type “a”
		{11}	Debug Data Type “b”
[24]	Transverse Parity (Parity of [0:23])		
[25:27]	Control	{111}	This is the first frame

This is redundant information, but it simplifies tracking of information

Frame 2

[28:31]	Number of Low PS Clusters Matched		
[32:35]	Number of High PS Clusters Matched		
[36:39]	Number of Low PS Clusters not Matched		
[40:43]	Number of High PS Clusters not Matched		
[44:51]	Null	{00000000}	
[52]	Transverse Parity (Parity of [28:51])		
[53:55]	Control	{000}	This is not the first frame

Bit Fields allocation for L1 FPS data transfers between the Collector Boards (U/V Boards) and the Broadcaster Board (L1 Trigger Terms) using LVDS Links



NOTE The Maximum number of Matched or Unmatched Clusters reported per Collector board is 31 for a theoretical maximum of 96.
Each data frame corresponds to a Quadrant.

Bit Fields allocation for L1 FPS data transfers between the Collector Boards (U/V Boards) and the Broadcaster Board (L1 Trigger Terms) using LVDS Links

Frame 1

Bits			
[0:7]	Data type	{10100101} = L1FPS	
[8]	Set to 1 if the PS strips have V orientation		This is redundant information, but it simplifies tracking of information
[9]	Set to 1 if the PS strips have U orientation		
[10]	Set to 1 for the South half		
[11]	Set to 1 for the North half		
[12:15]	The Relative Address of Sector in the North/South half		
[16:21]	Null	{000000}	
[22:23]	Pass and Mark	{00}	Normal Data, Normal Event
		{01}	Normal Data, Pass Event (unbiased data)
		{10}	Debug Data Type “a”
		{11}	Debug Data Type “b”
[24]	Transverse Parity (Parity of [0:23])		
[25:27]	Control	{111}	This is the first frame

Frame 2

[28:30]	Null	{000}	
[31:35]	Number of Low PS Clusters Matched		**First Quadrant**
[36:40]	Number of High PS Clusters Matched		
[41:45]	Number of Low PS Clusters not Matched		
[46:50]	Number of High PS Clusters not Matched		
[51]	Null	{0}	
[52]	Transverse Parity (Parity of [28:51])		
[53:55]	Control	{000}	This is not the first frame

Bit Fields allocation for L1 FPS data transfers between the Collector Boards (U/V Boards) and the Broadcaster Board (L1 Trigger Terms) using LVDS Links

	Bits			
Frame 3	[56:58]	Null	{000}	
	[59:63]	Number of Low PS Clusters Matched		
	[64:68]	Number of High PS Clusters Matched		**Second Quadrant**
	[69:73]	Number of Low PS Clusters not Matched		
	[74:78]	Number of High PS Clusters not Matched		
	[79]	Null	{0}	
	[80]	Transverse Parity (Parity of [56:79])		
	[81:83]	Control	{000}	This is not the first frame
Frame 4	[84:86]	Null	{000}	
	[87:91]	Number of Low PS Clusters Matched		
	[92:96]	Number of High PS Clusters Matched		**Third Quadrant**
	[97:101]	Number of Low PS Clusters not Matched		
	[102:106]	Number of High PS Clusters not Matched		
	[107]	Null	{0}	
	[108]	Transverse Parity (Parity of [84:107])		
	[109:111]	Control	{000}	This is not the first frame

Bit Fields allocation for L1 FPS data transfers between the Collector Boards (U/V Boards) and the Broadcaster Board (L1 Trigger Terms) using LVDS Links

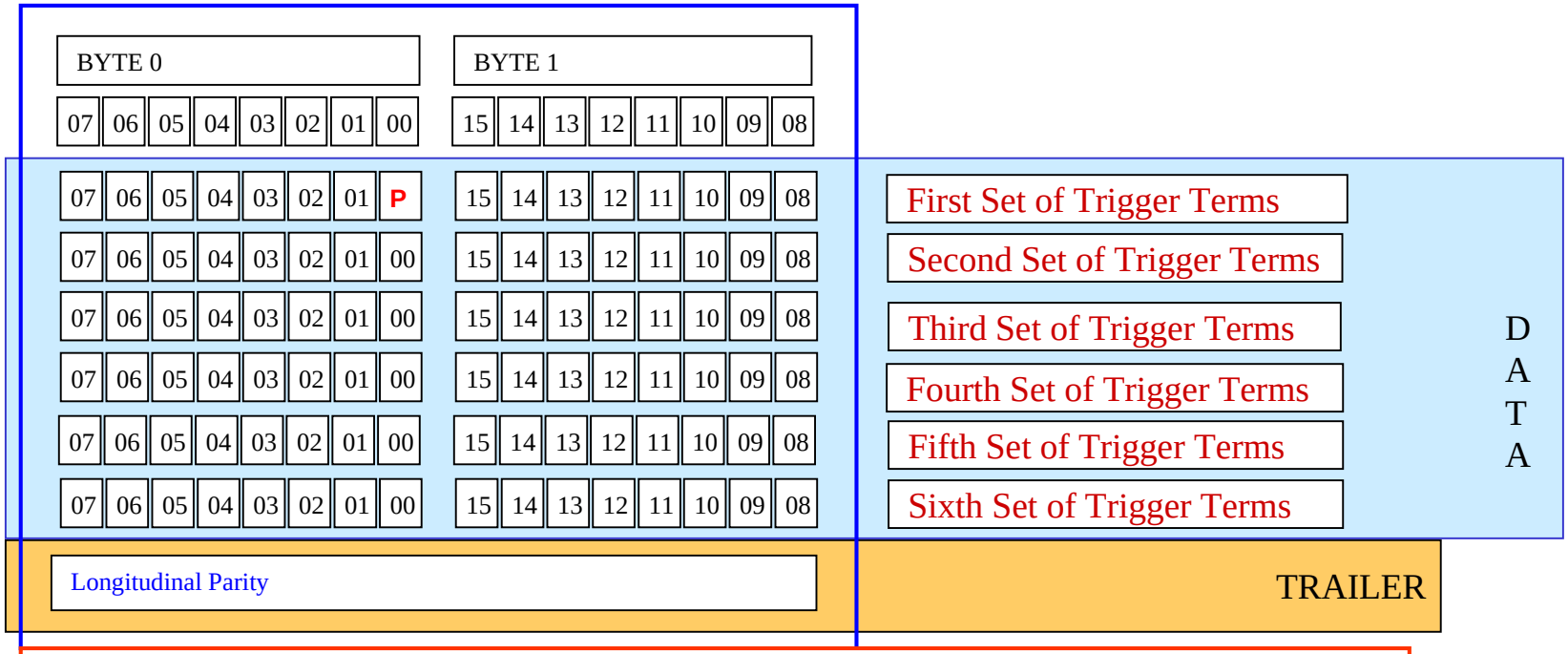
Frame 5

Bits			
[112:114]	Null	{000}	
[115:119]	Number of Low PS Clusters Matched		
[120:124]	Number of High PS Clusters Matched		**Fourth Quadrant**
[125:129]	Number of Low PS Clusters not Matched		
[130:134]	Number of High PS Clusters not Matched		
[135]	Null	{0}	
[136]	Transverse Parity (Parity of [112:135])		
[137:139]	Control	{000}	This is not the first frame

Frame 6

[140:163]	Null	{00}	
[164]	Transverse Parity (Parity of [140:163])		
[165:167]	Control	{000}	This is not the first frame

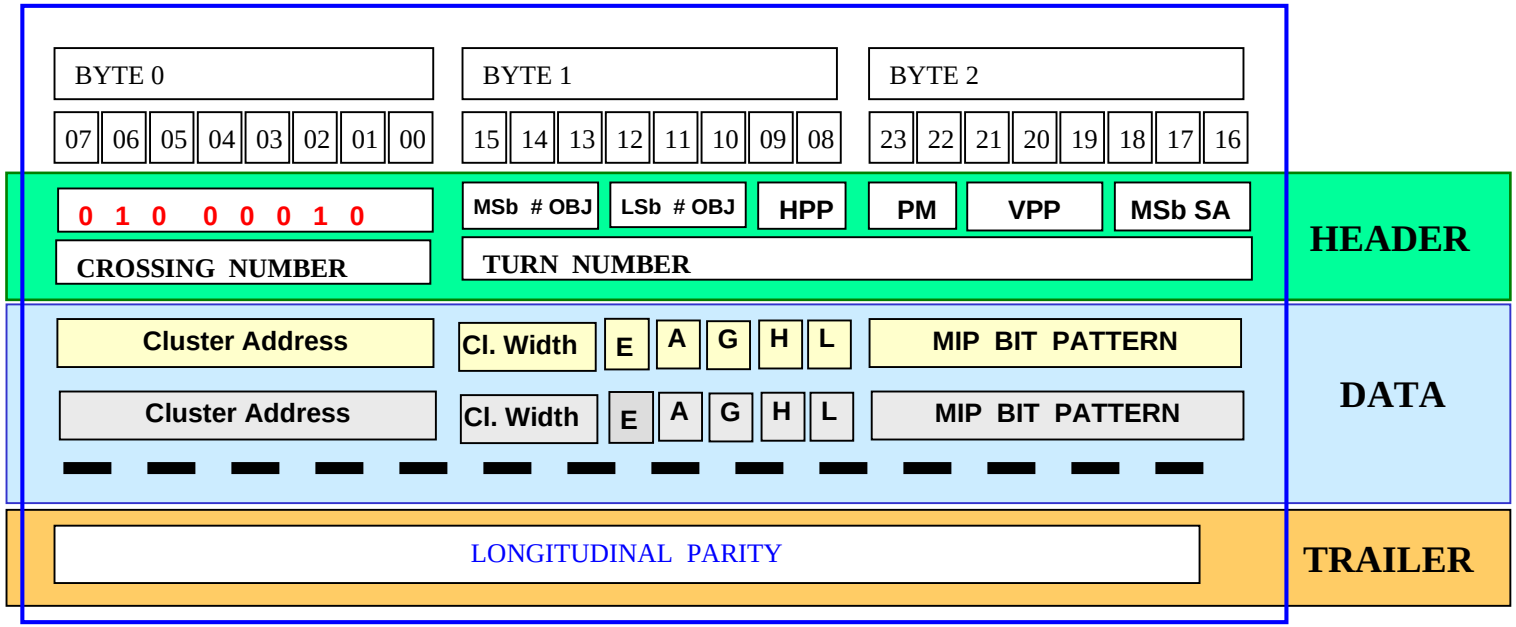
Bit Fields allocation for L1 FPS data transfers between the Broadcaster Board (L1 Trigger Terms) and the Trigger Manager using FSC Links



NOTE P=1 if it is a Pass and Mark event

This board can define up to 96 Trigger Terms and send them to a Trigger Manager Board. The Trigger Manager Selects 48 from the List to send to the Trigger Framework

Bit Fields allocation for L2 FPS data transfers between the Digital Front End boards and the Collector Boards using LVDS Links



NOTES The Maximum number of Clusters reported per 22.5^0 Wedge is 16 from each side (N/S)

The Cluster List is ordered in increasing strip index

Glossary of terms

Data Type	What Type of data (CFT, CPS, etc).
MSb # OBJ	The three Most Significant bits of the number of Data Frames carrying data. It does not include Header or Trailer frames.
LSb # OBJ	The three Least Significant bits of the number of Data Frames carrying data. It does not include Header or Trailer frames.
LSb SA	The four Least Significant bits of unique number identifying the geographical position of the "source" of the data.
MSb SA	The three Most Significant bits of unique number identifying the geographical position of the "source" of the data.
TM	Code for Pass and Mark and debugging.

Bit Fields allocation for L2 FPS data transfers between the DFE and the Collector Boards (U/V Boards) using LVDS Links

Frame 1

Bits			
[0:7]	Data type	{01000010} = L2FPS	
[8:9]	Horizontal Parity of the 2x3 matrix giving the # of Objects		
[10:12]	Less Significant bits of the # of Objects (first Row of the matrix address)		
[13:15]	Most Significant bits of the # of Objects (first Row of the matrix address)		
[16:18]	Vertical Parity of the 2x3 matrix giving the # of Objects		
[19:21]	Most Significant bits of the 4.5º Sector = Relative Address of the Octant		
[12:23]	Pass and Mark	{00}	Normal Data, Normal Event
		{01}	Normal Data, Pass Event (unbiased data)
		{10}	Debug Data Type “a”
		{11}	Debug Data Type “b”
[24]	Transverse Parity (Parity of [0:23])		
[25:27]	Control	{111}	This is the first frame

Frame 2

[28:35]	Crossing Number		
[36:51]	Turn Number		
[52]	Transverse Parity (Parity of [0:23])		
[53:55]	Control	{000}	This is not the first frame

Bit Fields allocation for L2 FPS data transfers between the DFE and the Collector Boards (U/V Boards) using LVDS Links

Frame 3

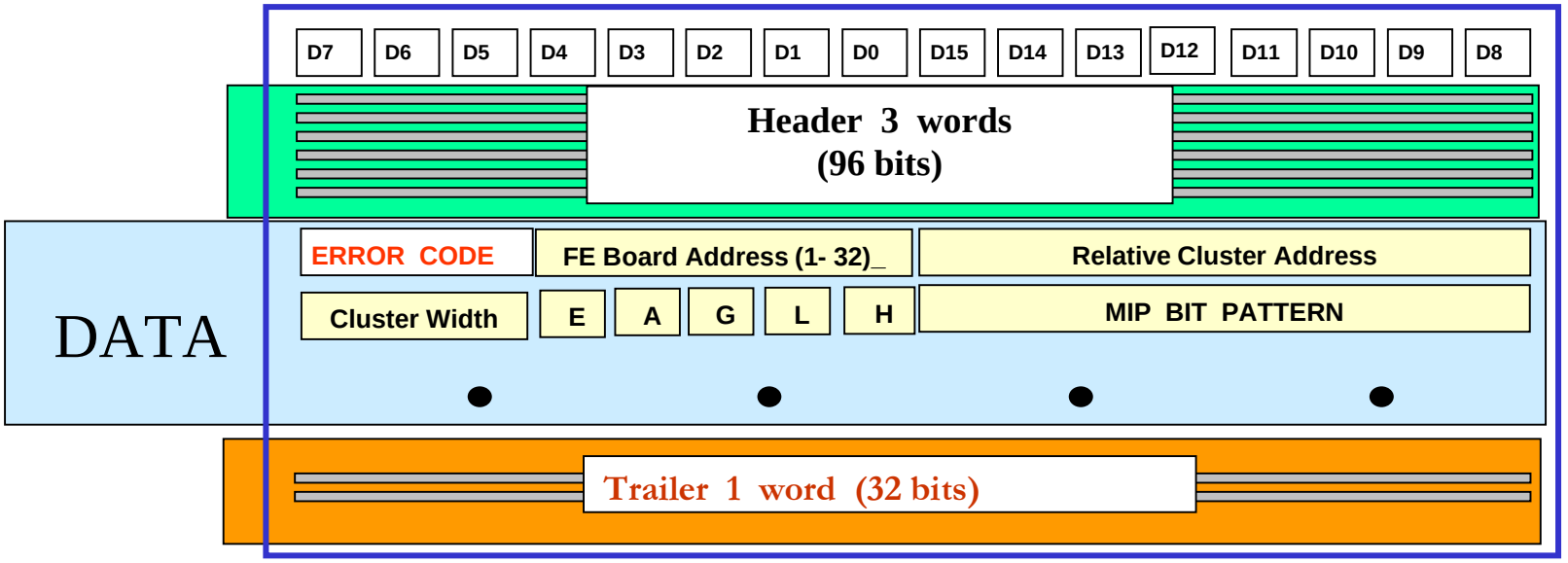
Bits			
[56:63]	Cluster Address (Relative Address of the First Strip of the Cluster)		
[64]	Set to 1 if it is a Low PS Cluster		
[65]	Set to 1 if it is a High PS Cluster		
[66]	North/South information		
[67]	Strip orientation (U/V)		
[68]	If set to 1 the Cluster defines an Electron Candidate		
[69:71]	Width of the Cluster		
[72:79]	MIP Bit Pattern		
[80]	Transverse parity (Parity of [56:79])		
[81:83]	Control	{000}	This is not the first frame

Frame n+3

(Longitudinal Parity)

[28*(n+2)]	Parity of [0, 28, 56, …, 28*(n+1)]		
[29*(n+2)]	Parity of [1, 29, 57, …, 29*(n+1)]		
*	* * * *		
*	* * * *		
[51*(n+2)]	Parity of [23, 51, 79, …, 51*(n+1)]		
[52*(n+2)]	Null	{0}	
[53*(n+2): 55*(n+2)]	Control	{000}	This is not the first frame

Bit Fields allocation for L2 FPS data transfers between the Collector Boards and the L2 PSpp (via FIC) using G Links



List of Clusters with tagging and address n*32 bits for a maximum of 48 Clusters per Collector board.
If truncation of data is necessary the reporting is done moving counter clock wise, this will result in a possible bias of the efficiency.

Meaning of Terms used

In this case the Header has only two Frames.

Each reported Cluster carries the following information

Cluster Address	The relative Address of the first element of the Cluster
Cluster Width	The number of elements in the Cluster
MIP BIT PATTERN	Pattern of 1s and 0s corresponding to the PS Strips Hits in a window in the MIP layer "in front" of the Shower layer cluster.
E	Set to 1 if the particle is an electron candidate
A	Orientation of the Cluster U/V
G	Set to 1 if North, set to 0 if South
H	If set the Cluster is a High Threshold PS Cluster
L	If set the Cluster is a Low Threshold PS Cluster